Innovation Grant
India Innovation Centre for Graphene, Kochi

India Innovation Centre for Graphene [IICG] announces Innovation Grant for **Graphene/2D Materials for Advanced Electronics and Photonics.**

1. Background

India Innovation Centre for Graphene (IICG), is a pioneering initiative of Ministry of Electronics and Information Technology, Government of India and Government of Kerala along with Centre for Materials for Electronics Technology, Thrissur (C-MET), Digital University Kerala (DUK) in Trivandrum, and Tata Steel Limited (TSL) as the implementation agencies and Maker Village & Kerala Startup Mission as the supporting partners. The application domains of the IICG will be developed with the support of industry partners, including startups at Maker Village, and within the Kerala Startup Mission ecosystem.

2. Aim

To conduct the IICG Innovation Grant which will produce accelerated output for the research topic "**Graphene/2D Materials for Advanced Electronics and Photonics**". The winning participants will be incubated as startups in IICG.

3. Innovation Grant Statement

Broad Area: Graphene/2D Materials for Advanced Electronics and Photonics

Problem Statement 1:

Title: Development of 2D Transition Metal Dichalcogenide (TMDC) and/or Graphene-Based CMOS-Compatible Image Sensors and Advanced Photodetectors

Introduction:

Two-dimensional (2D) materials such as TMDCs (MoS_2, WS_2) and graphene offer groundbreaking optical and electrical properties for next-generation photodetectors and image sensors. However, most developments remain trapped at the level of isolated, individual flakes in academic labs.

This Innovation Grant focuses on bridging that gap by advancing the technology to at least Technology Readiness Level (TRL) 4. The goal is to move from isolated material testing to

demonstrating a component-level, functional prototype where 2D material sensing elements are successfully integrated with a basic CMOS readout platform.

The challenge is to design, fabricate, and validate a working laboratory-scale 2D photodetector array that meets core performance benchmarks against standard silicon technology. The proposal should focus on achieving high photoresponsivity and detectivity, fast response and recovery times, low dark current, and improved signal-to-noise ratios through suitable device design, material selection, and integration strategies.

Innovation Objectives:

1. Material Integration:

- Engineer reproducible 2D heterostructures optimized for photoresponse, charge collection, and spectral sensitivity.
- Demonstrate component-level integration by bonding or interfacing the 2D sensing elements with a basic CMOS readout platform.

2. Core Performance & Initial Array Prototyping:

- Fabricate and test a small-area pixel array (targeting an initial 8 x8 pixel array or a workable subset, depending on readout feasibility) to show basic spatially resolved imaging capability.
- Achieve foundational electrical and optical targets under calibrated lab testing:
    - **Photoresponsivity:** ≥ 0.1 to 10^3 A/W (based on the application which should be specified)
    - **Specific Detectivity:** $\geq 10^9$ Jones
    - **Response Time:** ≤ 10 ms

3. Laboratory Testing & Benchmarking:

- Evaluate baseline device-to-device reproducibility, dark current, and noise performance in a controlled lab environment.
- Conduct preliminary stress/stability tracking, aiming for $\geq 90\%$ responsivity retention after initial controlled testing.
- Directly benchmark the laboratory prototype against conventional silicon photodiodes and CMOS reference devices under equivalent measurement conditions to prove tangible improvements in dark current, noise floor, and signal-to-noise ratio.

Additionally, the proposer should closely work with C-MET/IICG to explore integration of materials developed by C-MET/IICG in to the device. Timelines and Milestones with predefined

deliverables and targeted TRL should be included in the proposal.
NOTE: The technical details for the evaluation including Design aspect, Targeted specifications, Timeline, TRL, Bench marking, Strategies, etc need to be clearly mentioned, without which the proposal will be not considered for the evolution.

Problem Statement 2:

Title: Development of Scalable 2D-Material based Field-Effect Transistors (FETs) for Post-Silicon Electronics

Introduction:
As traditional silicon technology approaches its fundamental physical scaling limits, the electronics industry urgently needs alternative channel materials to sustain performance growth. Two-dimensional (2D) materials such as atomically thin transition metal dichalcogenides (TMDCs like (MoS_2, WS_2) and graphene offer ultimate thickness control, high carrier mobility, and unique electrical properties.

However, moving from isolated academic flakes to a validated, component-level 2D transistor remains a massive hurdle due to high contact resistance, interface trap states, and fabrication variability.

This Innovation Grant focuses on advancing 2D FET technology to Technology Readiness Level (TRL) 4. The goal is to design, fabricate, and laboratory-validate a high-performance 2D material-based FET architecture that demonstrates competitive electrical switching and addresses traditional bottleneck issues like contact resistance and subthreshold swing.

Innovation Objectives:

1. **Material Growth & Contact Engineering**
    - **Channel & Dielectric Integration:** Utilize uniform 2D semiconductor channels (e.g., CVD-grown MoS_2 or layered high-κ dielectrics) to minimize defect density ($N_T < 10^{12}$ cm^{-2})
    - **Contact Optimization:** Implement strategies to minimize parasitic metal-semiconductor contact resistance, targeting specific contact resistance ≤ 1 kΩ.μm

2. **Device Fabrication and Prototyping**
    - **Device Prototyping:** Fabricate back-gated or top-gated 2D FET arrays on scalable substrates (e.g., 2-inch/4 -inch sapphire or silicon wafers).
    - **Core Electrical Targets (Subject to experimental validation):**
        - **On-Off Current Ratio** (I_{ON}/I_{OFF}): $\geq 10^6$ (for logic applications).
        - **Subthreshold Swing (SS):** Approaching closer to the thermionic limit ($\leq$ 100 mV/dec, with target optimization toward standard scaling behavior).
    - **Field-Effect Mobility** (μ_{FE})**:** Competitive baseline performance relative to state-of-the-art lab precursors for monolayer/few-layer TMDCs ($\geq$ 10 to 50 $cm^2/V.s$)
    - **On-State Current density** (I_{ON}): 10 to 100 μA/μm or better at a set drain-source voltage (eg. V_{DS} = 1 V)
    - **Threshold Voltage (V_{th}) Uniformity:** Minimal variation across the array (e.g., standard deviation < 100 mV)
3. **Reliability Testing & Silicon Benchmarking**
    - **Hysteresis & Stability Control:** Mitigate charge-trapping and environmental hysteresis under repeated voltage sweeps, demonstrating stable transfer characteristics over repeated test cycles.
    - **Comparative Benchmarking:** Benchmark the electrical output characteristics, drain current density (I_D), and transconductance directly against baseline silicon-based or conventional thin-film reference transistors under equivalent measurement protocols.

Additionally, the proposer should closely work with C-MET/IICG to explore integration of materials developed by C-MET/IICG in to the device. Timelines and Milestones with predefined deliverables and targeted TRL should be included in the proposal.

NOTE: The technical details for the evaluation including Design aspect, Targeted specifications, Timeline, TRL, Bench marking, Strategies, etc need to be clearly mentioned, without which the proposal will be not considered for the evolution.

Problem Statement 3:

Title: Development of Graphene/2D Material-Based Chemiresistive Gas Sensors for Automotive Applications

Introduction:

Automotive systems require reliable gas detection to improve occupant safety, cabin air quality, emission monitoring and early identification of hazardous conditions. Conventional gas sensors face challenges such as cross-sensitivity, high operating temperature, humidity interference, drift, limited miniaturization or power consumption, depending on the sensing technology.

The Innovation Grant looks for proposals to develop compact, low-power, highly sensitive and selective chemiresistive gas sensors using graphene and other two-dimensional (2D) materials for automotive applications at Technology Readiness Level (TRL) 5. The sensor must exhibit high selectivity, long-term stability, response recovery and performance under automotive environmental conditions, alongside compatibility with miniaturized sensor fabrication which must be demonstrated before practical deployment.

The project will address these challenges through material engineering, sensor-array design, signal processing, environmental compensation and validation in a simulated automotive environment.

Innovation Objectives:

Development of Graphene/2D Material-Based Chemiresistive Gas Sensors for Automotive Applications:

- **Material innovation:** Specify the exact 2D material system. Detail the material's synthesis route and how the properties will be tailored to ensure high performance sensors.
- **Sensor Configuration & Integration:** Brief architecture detailing sensor configuration and integration of readout electronics, signal-to-noise ratio optimization, etc.
- **Stability and Reliability:** Technical proof of concept outlining how the device will mitigate degradation or baseline drift over extended operation in different environments
- **Target gases:** NO_2 (0.1-10 ppm), CO (1-100 ppm), NH_3 (1-50 ppm), H_2 (10-1000 ppm) and selected VOCs (1-100 ppm) in automobile.
- **Target detection repeatability**: ≤10% relative variation under controlled conditions
- **Operating environment**: Ambient sensing temperature (-20 to 85°C), 10-95% RH.
- Automotive vibration and electrical-transient testing appropriate to the intended mounting location.

- **Electronics and interface**: Target supply 9–16 V DC for a 12 V vehicle system, Target module power: ≤1 W, subject to heater requirements.
- **Scalability Strategy:** A concrete plan demonstrating how the proposed sensor can be transitioned from lab-scale level to high-throughput, repeatable fabrication for mass production
- **Deliverables and Milestones:** A rigorous project execution framework with predefined deliverables and milestones with targeted Technology Readiness Level (TRL)

Participants need to submit ideas, designs, product plans, or prototypes of their proposed solutions.

Additionally, the proposer should closely work with C-MET/IICG to explore integration of materials developed by C-MET/IICG in to the device.

Timelines and Milestones with predefined deliverables and targeted TRL should be included in the proposal.

NOTE: The technical details for the evaluation including Design aspect, Targeted specifications, Timeline, TRL, Bench marking, Strategies, etc need to be clearly mentioned, without which the proposal will be not considered for the evolution.

Problem Statement 4:

Title: Design and development of complete electronic module for 2D array/Graphene/piezo based material for next generation underwater transducer

Introduction:

C-MET, through IICG, is developing 2D array/Graphene/piezo based materials for underwater transducer for imaging applications. Though the material used for underwater transducer could be 2D array/Graphene/piezo based material, there is a challenge to develop the associated electronics for underwater imaging. For compete realization of Underwater system for viewing and imaging applications, the transducer elements along with associated electronics needs to be developed. For the current problem statement, transducers will be provided by C-MET as per the required frequency range. The grant challenge will involve design and development of complete electronics

module for the next generation underwater transducer with the following broad minimum specifications.

The specifications and Performance Targets of the challenge

Transducer specification:

- Transducer material: 2D array/Graphene/piezocomposites
- Broad frequency range: 700 kHz- 1.00 MHz
- Operating range: 0.75 m – 100 m
- Bandwidth: Narrow (Horizontal beamwidth: 2-10^{o}, Vertical bandwidth: 25 - 40^{o})
- Maximum depth rating: 300 m
- Range resolution: Upto 0.1% of the selected range

Electronic module specification

The complete electronics module may consist of two PCB sections, first section consists of electronics required for transmission and receipt of underwater pulse-echo signals while the other PCB consist of electronics required for data transmission to Automated Surface vehicles (ASVs). The minimum specifications for the complete electronics module are described as follows:

- Time of flight: 0.7 milliseconds – 0.2 sec (for the round trip from the distance to target)
- Receiving Sensitivity: - 100 dB to -200 dB re 1V/µPa
- Supply voltage: 11 V to 25 V DC
- Data transfer speed: 60 kbps to 100+ kbps
- Power consumption: 5 - 10 W while underwater scanning
- Scan range: Variable upto 360 ^{o}
- Scan speed: ~10 sec at 2m range and ~80 sec at 100m range
- Communication protocol: USB/Ethernet/RS-485
- Form factor: Needs to be designed in such a way that the complete electronics module can be handheld.

The above specifications are mainly meant for the electronics module configuration intended for underwater transducer applications. We would expect proposals with upgraded specifications for 2D array/Graphene/piezo based material. The developed circuit should be demonstratable in the above-mentioned frequency range for underwater viewing or imaging.

Participants need to submit ideas, designs, product plans, or prototypes of their proposed solutions. The proposer should have prior experience in designing PCB circuits in relevant areas of

underwater transducer applications. At least 5 numbers of complete electronics modules demonstratable as per above specifications should be provided as deliverables. The proposer should closely work with C-MET for understanding the components in the required frequency range etc. for underwater imaging applications. C-MET/IICG, at its discretion, will do the field trials with any of IICG/C-MET's partners for validating the samples.

Time lines and milestones with predefined deliverables and targeted Technology Readiness Level (TRL) should be included in the proposal. Additionally, the proposer should closely work with C-MET/IICG to explore integration of materials developed by C-MET/IICG in to the device.

NOTE: The technical details for the evaluation including Design aspect, Targeted specifications, Timeline, TRL, Bench marking, Strategies, etc need to be clearly mentioned, without which the proposal will be not considered for the evolution.

Prize Money and funding

- For each problem statement maximum up to **Rs 25 lakhs** and free incubation. Aspirants can apply for multiple problem statements. All the IP in this respect will rest with IICG.
- **Duration of Innovation Grant: Maximum 01 Year**

The proposals need to be submitted as per the format to innovationgrant.iicg@gmail.com
Application link:
https://drive.google.com/file/d/1dLeY-ApVgDhrB5xlhI3V1tmdGp9g1Gpn/view?usp=drive_link

2. Eligibility Criteria

- The call is open for all Indian Academic Institutes / Research Institutes / Start-ups / Entrepreneurs

3. Implementing Agency

- The implementing agency will be the IICG, Kochi.

4. Evaluation Methodology

- **Level 1: Screening** - The proposal will be screened based on its merits.
- **Level 2: Presentation** - Shortlisted candidates will be called for presentation for final selection.

5. Important date to be noticed

- Submission last date: 26 Nov, 2026
- More information on: https://www.graphenecentre.in, and https://cmet.gov.in/

6. Rule and Guidelines

a. All participants and team have to be eligible (See Eligibility Criteria) to participate.
b. During the Innovation Grant, the Team Leader shall be considered as the Single Point of Contact for all engagements & communication by the IICG. Furthermore, the Team Leader cannot be changed during the course of the Innovation Grant.
c. The Team Leader and Team Members will be required to provide working E-mail IDs and Mobile numbers for the purpose of Registration/ Communication.
d. Teams shall maintain detailed documentation of their Idea, Prototype and Solution at all stages of the Innovation Grant for reference and record purposes.
e. The right to summarily reject any change in team composition is vested with IICG.
f. Any IPR if generated in the Innovation Grant shall be jointly owned by the IICG and the contributing team through a separate MoU as per Indian Laws/ Rules.
g. The solution should not violate/breach/copy any idea/concept/product already copyrighted, patented or existing in this segment of the market. Legal liability of such infringement will be the sole responsibility of the applicant team.
h. Anyone found to be non-compliant of rules and guidelines face the risk of their participation getting cancelled.
i. All documents/ papers etc submitted in relation to the Innovation Grant is non-returnable and shall remain as the property of IICG.
j. The number of teams to be finally selected and incubated or not to be selected at all is at the sole discretion of IICG and no suggestions and disputes will be entertained.
k. For any dispute redress, Secretary (MeitY)'s decision will be the final.
l. The selected teams receiving funding through this call have to give their written consent to must be willing to be incubated in the IICG.
m. Previous Innovation Grant winners are not eligible for applying the PRESENT Innovation Grant till the project is over.

Appendix 1

Technology Readiness Levels (TRL)

Technology Readiness Levels (TRL) are a method used to measure and assess the maturity of a particular technology

TRL is based on a scale from 1 to 9 with 9 being the most mature technology.

Leve l	Definition	TRL Description
1	Basic principles observed and reported	Lowest level of technology readiness. Scientific research begins to be translated into applied research and development. Examples might include paper studies of a technology's basic properties.
2	Technology concept and/or application formulated.	Invention begins. Once basic principles are observed, practical applications can be invented. Applications are speculative and there may be no proof or detailed analysis to support the assumptions. Examples are limited to analytic studies.
3	Analytical and experimental critical function and/or characteristic proof of concept.	Active research and development is initiated. This includes analytical studies and laboratory studies to physically validate analytical predictions of separate elements of the technology. Examples include components that are not yet integrated or representative.
4	Component and/or breadboard validation in laboratory environment.	Basic technological components are integrated to establish that they will work together. This is relatively "low fidelity" compared to the eventual system. Examples include the integration of "ad hoc" hardware in the laboratory.

5	Component and/or breadboard validation in relevant environment.	The Fidelity of breadboard technology increases significantly. The basic technological components are integrated with reasonably realistic supporting elements so it can be tested in a simulated environment.
6	System/subsystem model or prototype demonstration in a relevant environment.	A representative model or prototype system, which is well beyond that of TRL 5, is tested in a relevant environment. Represents a major step up in a technology's demonstrated readiness.
7	System prototype demonstration in an operational environment.	Prototype near, or at, planned operational system. Represents a major step up from TRL 6, requiring the demonstration of an actual system prototype in an operational environment such as an aircraft, vehicle, or space.
8	Actual system completed and qualified through test and demonstration.	Technology has been proven to work in its final form and under expected conditions. In almost all cases, this TRL represents the end of true system development. Examples include developmental test and evaluations of the system in its intended weapon system to determine if it meets design specifications.
9	Actual system has proven through successful mission operations.	The actual application of the technology in its final form and under mission conditions, such as those encountered in operational test and evaluation. Examples include using the system under operational mission conditions.

Appendix 2

Commercial Readiness Levels (TRL)

Commercial Readiness Levels (CRL) is a framework for defining the spectrum of commercial maturity, from basic market research to full deployment.

CRL is based on a scale from 1 to 9 with 9 being the most commercial technology.

CRL	Description
1	Knowledge of applications, use-cases, & market constraints is limited and incidental, or has yet to be obtained at all.
2	A cursory familiarity with potential applications, markets, and existing competitive technologies/products exists. Market research is derived primarily from secondary sources. Product ideas based on the new technology may exist, but are speculative and unvalidated.
3	A more developed understanding of potential applications, technology use-cases, market requirements/constraints, and a familiarity with competitive technologies and products allows for initial consideration of the technology as product. One or more "strawman" product hypotheses are created, and may be iteratively refined based on data from further technology and market analysis. Commercialization analysis incorporates a stronger dependence on primary research and considers not only current market realities but also expected future requirements.
4	A primary product hypothesis is identified and refined through additional technology-product-market analysis and discussions with potential customers and/or users. Mapping technology/product attributes against market needs highlights a clear value proposition. A basic cost-performance model is created to support the value proposition and provide initial insight into design trade-offs. Basic competitive analysis is carried out to illustrate unique features and advantages of technology. Potential suppliers, partners, and customers are identified and mapped in an initial value-chain analysis. Any certification or regulatory requirements for product or process are identified.

5	A deep understanding of the target application and market is achieved, and the product is defined. A comprehensive cost-performance model is created to further validate the value proposition and provide a detailed understanding of product design trade-offs. Relationships are established with potential suppliers, partners, and customers, all of whom are now engaged in providing input on market requirements and product definition. A comprehensive competitive analysis is carried out. A basic financial model is built with initial projections for near- and long-term sales, costs, revenue, margins, etc.
6	Market/customer needs and how those translate to product needs are defined and documented (e.g. in market and product requirements documents). Product design optimization is carried out considering detailed market and product requirements, cost/performance trade-offs, manufacturing trade-offs, etc. Partnerships are formed with key stakeholders across the value chain (e.g. suppliers, partners, customers). All certification and regulatory requirements for the product are well understood and appropriate steps for compliance are underway. Financial models continue to be refined.
7	Product design is complete. Supply and customer agreements are in place, and all stakeholders are engaged in product/process qualifications. All necessary certifications and/or regulatory compliance for product and production operations are accommodated. Comprehensive financial models and projections have been built and validated for early stage and late stage production.
8	Customer qualifications are complete, and initial products are manufactured and sold. Commercialization readiness continues to mature to support larger scale production and sales. Assumptions are continually and iteratively validated to accommodate market dynamics.
9	Widespread deployment is achieved.